Remarks/Arguments

Claims 1-9 are pending.

Rejection of claims 1-9 under 35 USC 103(a) as being unpatentable over Brunherto et al. (US Pat No 6654389) in view of Adachi et al. (US Pat No 6115425)

Applicants submit that for the reasons discussed below present claims 1-9 are patentably distinguishable over the combination of Brunherto et al and Adachi et al.

The office action asserts that Brunherto differs from the claimed invention in that Brunherto does not specifically teach the step of carrying out a modulo-n counting of the data blocks in order to determine the data source packet boundaries, and in that the beginning of a new data source packet is signaled to a memory management device at the beginning of the next counting interval. Applicants submit that as discussed below Brunherto also fails to teach other elements of the claimed invention.

Claim 1 recites "... receiving data transmitted in bus packets having a variable length, each bus packet having a header and a payload data field, **the payload data field being divided into data blocks having a defined length, a combination of a defined number n of data blocks forming a data source packet of fixed length,** section-by-section transmission of the data source packet within the framework of data blocks being permitted..." (emphasis added) Applicants submit that Brunherto fails to disclose or suggest this limitation of claim 1.

The Office Action alleges that Brunherto discloses bus packet having a header and a payload data field as recited in claim 1. In support, the Office Action refers to item 75 of figure 2.

Applicants respectfully submit that the Office Action misapplies the teachings of Brunherto. Item 75 of figure 2 is clearly identified as a transport packet 9 (col. 4, line 62). As is well known by those skilled in the art, transport packets have a defined length of 188 bytes (col. 1, lines 29-32). Therefore, packet 75 cannot correspond to the recited bus packets having a variable length.

Figure 2 of Brunherto also shows a TDM slot 73 which may include portions of packet 75. Brunherto appears to teach that TDM slot 73 may have variable size and include a header field 72. It also appears from figure 2 that the length of packet 75 is greater than the length of slot 73, and thus, packet 75 needs to be segmented into portions to be carried in the TDM slots. However, Brunherto is silent as to how such segmentation should be done.

By contrast, claim 1 recites: "... the payload data field being divided into data blocks having a defined length, a combination of a defined number n of data blocks forming a data source packet of fixed length..." The recited segmentation of the packet into fixed length data blocks is not taught or suggested in Brunherto. The cited passage on col. 6, line 35 to col. 8, line 41 describes an example where a 100 Mbyte file is transferred in 64K segments. The 64K units are segmented into 188 byte units of the transport packet. A further segmentation of the MPEG-2 packets into a number of fixed length blocks is not taught or suggested by Brunherto.

In view of the above, applicants submit that Brunherto fails to disclose or suggest dividing the payload data field of a bus packet into a number of data blocks having a fixed length, where a combination of defined number of n of data blocks forms a data source packet of fixed length.

The office action acknowledges that Brunherto fails to teach or suggest the step of "... carrying out a modulo-n counting ..." Adachi is cited as teaching the step of carrying out a modulo-n counting of the data blocks to determine the data source packet boundaries. Applicants disagree that Adachi teaches this feature and submit that Adachi fails to disclose or suggest the claimed segmentation of a data source packet into fixed length blocks.

Adachi relates to a block encoder/decoder comprising a circuit in which variable length coded data is distributed over fixed length sections where a partly filled section is filled up with data of a block having data in excess of the section length. However, Adachi does not show segmentation of a source packet having fixed length into a number of fixed length blocks. Applicants submit that the variable length blocks cannot be read to correspond to the claimed data source packets of fixed length.

Further, Applicants respectfully submit that there is nothing in Adachi to suggest a modulo-N counting of fixed length data blocks for the purpose of finding the source packet boundaries of a source packet consisting of a fixed number of fixed length data blocks.

Specifically, Adachi relates to a variable length coded data transmission device for use in a block encoder/decoder. The variable length blocks shown in Fig. 2 are distributed over fixed length slots, where the beginning of a variable length block is always at the beginning of a fixed length data slot. When a variable length data block has data for more than a fixed length data slot, the remaining data will be distributed over the following fixed length data slots having unoccupied data capacity.

This is done in a manner that the data of an ith variable length block is started to fill in the ith slot. If all of the data of the variable length block does not fit in the ith slot, the remaining portion of the block is shifted to some unoccupied space of the next slot provided that there is some unoccupied space in the slot. Otherwise the slot following the next slot will be filled, etc. The method implies that in some of the N slots there is some unoccupied space.

In the present invention, the modulo-n counting is used for determining data source packet boundaries. Adachi is not concerned with data source packet boundary determination. Nowhere does Adachi teach or suggest that the variable length data block is divided in fixed length blocks. Nowhere does Adachi teach or suggest that variable length packets divided in fixed length blocks will be transmitted over a serial bus in bus packets of variable length in units of the fixed length data blocks.

In view of the above, applicants submit that the combination of Brunherto and Adachi fail to teach or suggest all of the limitations of claim 1, and as such, claim 1, and claims 2-4 that depend therefrom, are patentably distinguishable over the cited combination.

Claim 5 recites limitations similar to that of claim 1 in apparatus form. As such, claim 5, and claims 6-9, which depend therefrom, are believed to be patentably distinguishable over the combination of Brunherto and Adachi for at least the same reasons as those discussed above.

Rejection of claim 9 under 35 USC 103(a) as being unpatentable over Brunherto et al. (US Pat No 6654389) and Adachi et al. (US Pat No 6115425) and further in view of Hatae et al. (US Pat No 6679769)

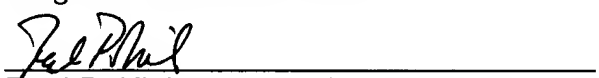
Hatae is cited as teaching the use of a bus according to the IEEE 1394 standard, where the apparatus is part of a data link layer moduel in the interface for the data bus. However, even assuming arguendo that Hatae teaches the above cited feature, applicants submit that Hatae fails to cure the defect of Brunherto and Adachi as applied to claim 5 as discussed above. Thus, claim 9, which depends from patentable claim 5, is believed to be distinguishable over the cited combination for at least the same reasons as those discussed with regard to Brunhero and Adachi.

Having fully addressed the Examiner's rejections, Applicants submit that the present application is in condition for allowance and respectfully request such action. No fee is believed due in regard to the present amendment. However, if a fee is due, please charge the fee to Deposit Account 07-0832. Should any questions arise regarding any of the above, the Examiner is requested to contact the undersigned at 609-734-6815.

Respectfully submitted,

PPK:lat

Siegfried Schweidler et al.

By: 

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